



UNITED STATES PATENT AND TRADEMARK OFFICE

S4
UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

09/783,598

02/15/2001

Kiyokazu Moriizumi

010153

4350

38834

7590

06/17/2004

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

EXAMINER

DINH, TUAN T

ART UNIT

PAPER NUMBER

2827

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n N . 09/783,598	Applicant(s) MORIIZUMI, KIYOKAZU	
	Examiner Tuan T Dinh	Art Unit 2827	

-- The MAILING DATE of this communication appears on th cover sheet with the correspondenc address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) 7-16 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Dat . _____. |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____. | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by

Nakahara (JP 04099372A, hereafter JP).

As to claim 1, JP discloses a front-and-back electrically conductive substrate having an insulation material (1) as shown in figures 1-3 comprising:

a plurality of posts (5) composed of a material that can be anisotropically etched, see an abstract, and each having an electrically conductive portion (7) that has at least first and second surfaces that communicate with each other; and an insulative substrate (1) that supports the plurality of posts (5).

As to claim 2, JP discloses in figure 2f the electrically conductive portion (7) comprises an electrically conductive film (see figure 6) covering a peripheral surface of the posts (5).

As to claim 3, JP discloses the insulative substrate (1) is composed of either ceramic, glass, or an organic resin (because it is a semiconductor substrate); and the

Art Unit: 2827

electrically conductive portion (7) is a metal having a melting temperature higher than a baking temperature or a melting temperature of an insulation used in the insulative substrate (1) because, the metal having a melting temperature higher than an insulative material.

As to claim 4, JP further comprising a pad (9) for mounting a semiconductor component (not shown) is formed on at least the first surface of the front and-back electrically conductive substrate.

As to claim 5, JP further comprising a thin film (9) composed of a wiring pattern layer and an insulation layer (8) is formed on at least the first surface of the front-and-back electrically conductive substrate, see figures 2-3.

3. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Otagawa et al. (U. S. Patent 5,294,504).

As to claim 1, Otagawa discloses a front-and-back electrically conductive substrate (silicon wafer, see column 8, line 10, and figures 1-10) having an insulation material comprising:

a plurality of posts (silicon posts, column 8, line 15) composed of a material (silicon material) that can be anisotropically etched (column 8, line 10), and each having an electrically conductive portion (platinum layer) that has at least first and second surfaces that communicate with each other; and an insulative substrate (silicon substrate of the wafer) that supports the plurality of posts.

As to claim 2, Otagawa discloses in figure 10 the electrically conductive portion (platinum layer) comprises an electrically conductive film covering a peripheral surface of the posts (silicon posts).

As to claim 3, Otagawa discloses the insulative substrate (1) is composed of either ceramic, glass, or an organic resin; and the electrically conductive portion (platinum layer) is a metal having a melting temperature higher than a baking temperature or a melting temperature of an insulation used in the insulative substrate (1) because, the metal having a melting temperature higher than an insulative material (silicon material).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Otagawa et al. ('504) in view of (JP'372A).

Otagawa does not disclose a pad or a thin film composed of a wiring pattern and a insulation layer formed on a first surface of the substrate.

As to claim 4, JP further comprising a pad or a thin film (9) composed of a wiring pattern layer and an insulation layer (8) is formed on at least the first surface of the front-and-back electrically conductive substrate, see figures 2-3.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a pad or a thin film and an insulation layer on a first surface of a substrate in the substrate of Otagawa et al, as taught by JP, in order to form an electrical connection and reducing heat for the substrate.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over JP('372A) or Otagawa et al. (504) in view of Onishi et al. (U. S. Patent 5,459,368).

As to claim 6, JP or Otagawa et al. do not show the insulation material of the insulative substrate having compensation of CTE different from the CTE of a mounted semiconductor component. However, Onishi et al. show a surface acoustic wave device mounted module in figure 1 comprising a surface acoustic wave element (1) made of at least one material selected from a group consisting of lithium niobate, lithium tannalate, lithium borate, and quartz, and an insulating resin multiplayer substrate (8), see column 4, lines 36-47. There is a compensate of different material between the multiplayer substrate and the element that would have different CTE therebetween.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the compensation of a different material having different CTE in the substrate of JP or Otagawa et al., as taught by Onishi et al., for the purpose of providing the sufficient melting temperature that applied on a component when mounted on a substrate.

R sponse to Argum nts

6. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Munakata (JP 0824591A) discloses a substrate having silicon posts, Shirakawa (JP 09205178A) discloses an insulation substrate having a plurality of polyimide resin posts, Thomas et al. (US Patent 4,379,979) discloses a silicon substrate having microposts, Kuist (US Patent 6,020,217) discloses semiconductor devices with CSP packages and method for making them, Document of application number 09/624,025, the document discloses a method of fabricating an IC isolation region comprising a step of anisotropically etching a substrate, Brambilla et al. (US Patent 6,350,671) discloses a method of antoaligning lines of a conductive material in IC on a semiconductor substrate.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2827

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Dinh
June 08, 2004.

Alonso Chambliss
Primary Examiner
AU 2827